

LOOK-AHEAD DECISION FEEDBACK EQUALIZING RECEIVER

Field of the Invention

5 The present invention relates to an I/O interface for use in communications between an SDRAM (synchronous dynamic random access memory) and a controller or between digital chips; and, more particularly, to an equalizing receiver which employs a look-ahead decision feedback equalizing
10 technology.

Background of the Invention

 The amount of data transmission as well as
15 transmission rate of the data in communications between a DRAM(dynamic random access memory) and a CPU(central processing unit) or between digital chips such as ASICs(application specific integrated circuits) continue to rise.

20 However, in such communications, the data transmission rate is limited by time jitter occurring in a PLL(phase locked loop)/DLL(delay locked loop) circuit, an offset due to dimensional deviations in the process of producing transmitters and receivers and so on. Also a setup/hold
25 time of a receiver circuit is not long enough, due to a reduction in a data size margin and a time margin resulting

from an inter-symbol interference (ISI) between signals. In such a case, the ISI is generated due to attenuation in high frequency components of signals in a transmission channel. Moreover, a time skew is generated, due to a difference in
5 time required for transmitting a signal through a channel, between signals or between a clock and the signal.

In the meantime, in order to transmit a signal at a high speed by overcoming a bandwidth limitation given in transmission channels of a bus structure where a plurality
10 of chips are interconnected through one conductive line, technologies for amplifying a high-frequency component of a signal in a transmitter or in a receiver have been developed.

The conventional technology for amplifying a high-frequency component of a signal in the transmitter is referred to as a pre-emphasis scheme, a structure thereof
15 being shown in Fig. 1. As shown in Fig. 1, the operation of the transmitter can be represented as

$$H(z) = 1 - a \cdot z^{-1} ,$$

so that it can serve as a high pass filter(HPF), wherein 'a' represents a constant and 'z' means a variable complex
20 number. The pre-emphasis scheme has usually been applied to current mode signaling circuits. However, since a SSTL (series stub terminated logic) channel for a DRAM interface employs a full-swing voltage-mode driving technique at a
25 transmitter output, it is difficult to use the pre-emphasis scheme for the SSTL channel.

The conventional technologies for amplifying a high-frequency component of a signal in the receiver are indicated in Figs. 2 and 3. The operation of the receiver in Fig. 2, i.e., a linear feed-forward scheme, can be
5 represented by

$$H(z) = 1 - a \cdot z^{-1} ,$$

wherein 'a' represents a constant and 'z' means a variable complex number. In the linear feed-forward scheme, a capacitor is required to store an input analog signal. In
10 this way, noise immunity of the receiver may be degraded due to the analog nature of the signal and an equalization circuit cannot be simplified due to the presence of analog storage circuits, e.g., capacitors.

Meanwhile, the operation of the receiver in Fig. 3, which is called as a decision feedback equalization (DFE)
15 scheme, can be represented by

$$Y[n] = x[n] - a \cdot \hat{Y}[n-1],$$

wherein 'n' is a positive integer, $x[n]$ represents a current external data signal fed to an equalizing amplifier, $\hat{Y}[n-1]$
20 indicates a preceding decision result, 'a' means a constant and $Y[n]$ shows an output voltage of the equalizing amplifier. In the DFE scheme, after it is determined whether a preceding external data signal $x[n-1]$ is H(High) or L(Low), a fraction of the preceding decision result, $a \cdot \hat{Y}[n-1]$, is
25 fed back to amplify a high-frequency component of the current external data signal. In contrast to the above-

mentioned linear analog feed-forward scheme, high noise immunity is achieved in the DFE scheme because of the digital nature of the feedback signal $a \cdot \hat{Y}[n-1]$ and an equalization circuit employing the DFE scheme may be much
5 simplified owing to the absence of analog storage circuits.

However, the DFE scheme has a limitation in a high-speed transmission due to a delay time at its feedback path. Furthermore, due to a difference in time required for transmitting signals through channels, there is a time skew
10 between transmitted signals or between a clock and a transmitted signal. The skew has an adverse effect on signal transmission at a high speed. For the normal operation of an input circuit in a receiver, a setup/hold time should be sufficient as needed, but the time skew makes
15 it difficult.

To solve the above-mentioned problems in the DFE scheme, the determination of suitable timing of a clock is required. For example, in the prior art, a proper sampling time is attained by over-sampling a transmitted signal (i.e.,
20 data are sampled twice or more per one period of the signal) for each data pin of a receiver. That is, in a 2X over-sampling scheme as shown in Fig. 4, the data of the signal are sampled three times in two periods of the signal, and if first two samples have a same value, the delay in the
25 sampling clock may increase. On the other hand, if last two samples have a same value, the delay time of the sampling

clock can be reduced. Through such a feedback procedure, a clock with a suitable delay (the timing of a sampling clock is determined to be in the middle of a specific portion of a stream of the data) is provided for each pin of the receiver.

5 In determining the suitable timing of a clock by using the 2X over-sampling scheme, a signal with minimal attenuation in time scale should be used. That is, if a high-frequency component of the signal is considerably attenuated while passing through a transmission channel, the
10 time uncertainty region of data is broadened, and the scheme for determining the suitability of the clock by using the over-sampling becomes ineffective due to an increase in time jitter. Thus, the 2X over-sampling scheme cannot be used in
15 a channel where a high-frequency component of a signal is seriously attenuated.

 In transmitting a signal in the above-mentioned digital system, therefore, there may occur various problems as further explained below.

20 First, when a signal is transmitted at a high speed in a channel of the digital system, a high frequency component of the signal may be attenuated. Such a phenomenon causes an ISI between signals and reduces a time margin and a voltage margin of the signal, thereby making it difficult to carry out data transmission at a high speed.

25 Secondly, in the prior art, in order to avoid such a phenomenon, an equalizing technology is applied to either a

terminal of a transmitter or that of a receiver, so that the attenuated component is compensated. However, the equalizing technology applied to the terminal of the transmitter is not applicable to a DRAM or an ASIC where a voltage at the terminal of the transmitter has a waveform of a full swing. Further, the equalizing technology applied to the terminal of the receiver has drawbacks such as low noise immunity and low-speed of data transmission.

Thirdly, when a clock signal is transmitted with a data signal from a transmitter to a receiver, a time skew is generated due to a difference in the delay time required for signals to pass through a transmission channel, which may in turn reduce the time margin of the data signal.

Fourthly, in order to solve the time skew problem, an over-sampling scheme is employed to find a suitable clock timing. However, in the occurrence of an attenuation of a signal, it is very difficult to apply such a scheme to a broadened time uncertainty region of the data signal.

Summary of the Invention

It is, therefore, a primary object of the present invention to provide an equalizing receiver, which adopts a look-ahead decision feedback equalizing scheme, for compensating an attenuation of a high-frequency component of a signal and further over-sampling the compensated signal so

that a skew between data and a clock is compensated, thereby facilitating a high speed data transmission.

In accordance with the present invention, there is provided a look-ahead decision feedback equalizing receiver including: an equalizing block for amplifying a high-frequency component of an external data signal fed thereto in response to a predetermined first input signal and a predetermined second input signal, to provide a first equalized external data signal and a second equalized external data signal, respectively; a clock synthesizer for outputting a plurality of sampling clocks, a timing thereof being adjusted by receiving an external clock synchronized with the external data signal; an over-sampler for over-sampling the first equalized external data signal and the second equalized external data signal in synchronization with the sampling clocks; a MUX block for multiplexing the outputs of the over-sampler in response to preceding outputs of the MUX block, which serve as select signals for the MUX block, to thereby attain MUX decision results; and a phase detector for deciding the timing of the sampling clocks by analyzing the MUX decision results.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following

description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 shows a conventional principle of an equalizing scheme employed in a transmitter;

5 Fig. 2 describes a conventional principle of an equalizing scheme employed in a receiver, which has no feedback loop;

10 Fig. 3 illustrates a conventional principle of an equalizing scheme employed in a receiver, which has a decision feedback circuit therein;

Fig. 4 offers a conventional principle of comparing a timing of a sampling clock with that of data by over-sampling;

15 Fig. 5 provides a block diagram of a receiver in accordance with a preferred embodiment of the present invention;

Fig. 6 presents a block diagram of an equalizing block, an over-sampler and a MUX block in accordance with the preferred embodiment of the present invention;

20 Fig. 7 depicts a circuit diagram of an equalizing amplifier and a sense amplifier D flip/flop in accordance with the preferred embodiment of the present invention; and

25 Figs. 8A and 8B represent circuit diagrams of a MUX even and a MUX odd, respectively, in accordance with the preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Fig. 5 is a block diagram illustrating a CMOS (complementary metal oxide semiconductor) receiver using a look-ahead decision feedback equalizing scheme in accordance with a preferred embodiment of the present invention. An external data signal with an attenuated high-frequency component is fed to an equalizing block 110 and an external clock signal synchronized with the external data signal is fed to a clock synthesizer 130. Herein, in case a DDR (double data rate) technology is applied to the receiver, the data transmission rates of the external data signal and the external clock signal are 2Gbps and 1GHz, respectively.

The equalizing block 110 equalizes the external data signals and provides the equalized signals to an over-sampler 120 which takes samples of the equalized external data signals at 0°, 90° and 180° phase sampling clocks provided by the clock synthesizer 130 (See Fig. 4 and clk0, clk90, clk180 in Fig. 5).

Then, the outputs of the over-sampler 120 are fed to a MUX (multiplexer) block 140 where the outputs of the over-sampler 120 are multiplexed, to thereby attain MUX decision results. The MUX decision results are decoded at a phase detector 150 to determine whether phases of the sampling clocks provided by the clock synthesizer 130 should be increased (or decreased) or not. Thus, the sampling clocks

are optimally synthesized by repeating the above-described procedure. Further, the external data signal is synchronized to the sampling clocks.

Fig. 6 shows a block diagram showing detailed structures of the equalizing block 110 including equalizing amplifiers 111 to 114, the over-sampler 120 including sense amplifier D flip/flops 121 to 128 and the MUX block 140 including a MUX even 141 and a MUX odd 142 in accordance with the present invention. Detailed circuit diagrams of the equalizing amplifier 111 and the sense amplifier D flip/flop 121 is represented in Fig. 7, and those of the MUX even 141 and the MUX odd 142 shown in Figs. 8A and 8B, respectively.

As shown in Fig. 6, a predetermined first input signal, i.e., a HIGH signal, is directly fed to input ports ein of equalizing amplifiers 111 and 113, and a predetermined second input signal, i.e., a LOW signal, is directly fed to input ports ein of equalizing amplifiers 112 and 114. Instead of the predetermined first and second input signals, it is also possible that the MUX decision results outputted from the MUX block 140 can be inputted to the equalizing amplifiers by feedback thereof. However, such a feedback structure causes decrease of the operational speed of the receiver. Therefore, in order to increase the speed of the receiver adopting the look-ahead decision feedback equalizing scheme in accordance with the present invention,

it is preferred that the predetermined first and second input signals are used instead of feed backing the MUX decision results.

5 Outputs of the equalizing amplifiers 111 and 112 in an even branch are sampled at the 0° and the 90° phase sampling clocks by the sense amplifier D flip/flops 121 to 124, and outputs of the equalizing amplifiers 113 and 114 in an odd branch are sampled at the 90° and the 180° phase sampling clocks by the sense amplifier D flip/flops 125 to 128.

10 Since, the outputs of the equalizing amplifiers are sampled at two sampling clocks for each of the branches, such a sampling operation is referred to as the 2X over-sampling. Among the outputs of the sense amplifier D flip/flops, H0 and L0 are acquired by sampling at the 0° phase sampling

15 clock, H90_1, L90_1, H90_2, L90_2 at the 90° phase sampling clock, and H180 and L180 at the 180° phase sampling clock. First characters H and L in the name of the outputs of the sense amplifier D flip/flops indicate that the corresponding outputs are acquired in case the High signal and the Low

20 signal are fed to the input ports ein of the equalizing amplifiers 111 to 114, respectively. Among these 8 outputs of the over-sampler 120, 4 outputs, which are going to be fed to the phase detector 150, are chosen in the MUX block 140.

25 The multiplexing operation of the MUX even 141 is performed in accordance with a signal o180, which is one of

output signals of the MUX odd 142. That is, if the signal o180 is High, H0 and H90_1 are chosen, and otherwise, L0 and L90_1 are chosen. Further, the multiplexing operation of the MUX odd 142 is executed in accordance with a signal o0,
5 which is one of output signals of the MUX even 141. That is, if the signal o0 is High, H90_2 and H180 are chosen, and otherwise, L90_2 and L180 are chosen. The outputs o0, o90_1, o90_2, o180 of the MUX block 140, which are called as the MUX decision results, are fed to the phase detector 150.
10 Further, as described above, the outputs o180 and o0 are also fed to select input ports (sels) of the MUX even 141 and the MUX odd 142, respectively.

The internal structures of the MUX even 141 and the MUX odd 142 are shown in Figs. 8A and 8B, respectively.

15 Referring to Fig. 8A, if a HIGH signal is fed to the select input port (sel) of the MUX even 141, a MUX 141a selects H0 among a first group including H0 and L0, and a MUX 141b selects H90_1 among a second group including H90_1 and L90_1. Otherwise, the MUX 141a selects L0 among the
20 first group, and the MUX 141b selects L90_1 among the second group. The signal selected from the first group and the signal selected from the second group are, respectively, sampled at D flip/flops 141c, 141d, which are synchronized with clk0, and then the sampled signals o0 and o90_1 are fed
25 to the phase detector 150.

Meanwhile, referring to Fig. 8B, in the first place,

H90_2 and L90_2 are, respectively, sampled at D flip/flops 142a and 142b, which are synchronized with clk0, and then fed to a MUX 142d, and H180 and L180 are fed to a MUX 142c, directly. And if a HIGH signal is fed to the select input
5 port (sel) of the MUX odd 142, the MUX 142c selects H180 among a third group including H180 and L180, and the MUX 142d selects the sampled H90_2 among a fourth group including the sampled H90_2 and the sampled L90_2. Otherwise, the MUX 142c selects L180 among the third group,
10 and the MUX 142d selects the sampled L90_2 among the fourth group. The signal selected from the third group and the signal selected from the fourth group are, respectively, sampled at D flip/flops 142e, 142f, which are synchronized with clk180, and then the sampled signals o180 and o90_2 are
15 fed to the phase detector 150.

The outputs o0, o90_1, o90_2, o180 of the MUX block 140 are fed to the phase detector 150, which outputs an up-signal (UP) or a down-signal (DOWN) in response to the outputs o0, o90_1, o90_2, o180 of the MUX block 140 as shown
20 in table 1. That is, clock delay is adjusted in accordance with the outputs of the MUX block 140 as shown in table 1. Thereafter, the up-signal and the down-signal are fed to the clock synthesizer 130 to thereby adjust a clock delay.

By repeating the above-mentioned procedure, the
25 circuit of Fig. 5 acquires the optimal sampling clock for sampling the external data signal, so that a high-speed

equalizing receiving operation can be achieved.

[Table 1]

o0, o90_1, o90_2, o180 (The outputs of the MUX block 140)	Clock Delay Adjustment
1100 or 0011	Fixed (delay is fixed)
1110 or 0001	Up (delay is increased)
1000 or 0111	Down (delay is reduced)

5 In accordance with the preferred embodiment of the present invention, the structure of the equalizing block 110 is divided into two branches, i.e., the even branch and the odd branch, and each of the branches is further diverged, each diverged portion corresponding to one of the
10 predetermined first and second input signals (HIGH, LOW), so that a plurality of the equalizing amplifiers 111 to 114 are required, as shown in Fig. 6.

 However, that is, not only since the purpose of diverging each branch is only for alleviating the effect of
15 noise and the like at a front end of the circuit of Fig. 6, but also since the outputs of the equalizing amplifiers 111 and 113 are same and the outputs of the equalizing amplifiers 112 and 114 are also same, only the equalizing amplifiers 111 and 112 or only the equalizing amplifiers 113
20 and 114 may be required. In this case, the output port of the equalizing amplifier 111 or 113 is fed to the over-samplers 121 and 122 in the even branch and the over-samplers 125 and 126 in the odd branch, and the output port

of the equalizing amplifier 112 or 114 is fed to the over-samplers 123 and 124 in the even branch and the over-samplers 127 and 128 in the odd branch.

5 While the invention has been shown and described with respect to the preferred embodiments, it will be understood by those skilled in the art that various changes and modifications may be made without departing from the spirit and the scope of the invention as defined in the following claims.

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